WHAT IS CLAIMED IS:

1. A semiconductor memory device including memory cells each having a trench capacitor and a fin-gate-type MOSFET that selects the trench capacitor, comprising:

a pillar formed on a major surface of a semiconductor substrate;

a device isolation region formed on the semiconductor substrate in a vicinity of a proximal portion of the pillar;

a gate electrode functioning as a word line, the gate electrode being formed on a side wall and an upper surface of the pillar;

a gate insulation film interposed between the pillar and the gate electrode;

a first activation region formed in the pillar and connected to a bit line;

a second activation region formed in the pillar and spaced apart from the first activation region such that the gate electrode is interposed between the second activation region and the first activation region;

a first oxide film formed on a side wall of the gate electrode, which corresponds to an upper surface of the pillar;

a trench formed in a vicinity of the second activation region in the pillar;

a capacitor formed on a side wall portion of the trench;

a second oxide film formed on the device isolation region at an upper part of the side wall of the pillar such that the second oxide film is located lower than the upper surface of the pillar; and

a surface strap formed on the second oxide film at a position above the second activation region in the pillar, the surface strap electrically connecting the second activation region and one of electrodes of the capacitor,

wherein insulation of the side wall of the gate electrode is effected by the first oxide film alone, insulation between the gate electrode and the surface strap is effected by the second oxide film alone, and contact between the surface strap and the second activation region is made at the upper surface and the side wall of the pillar.

2. The semiconductor memory device according to claim 1, further comprising a third oxide film buried at a side wall portion of the surface strap and formed of the same material as the second oxide film.

3. The semiconductor memory device according to claim 1, further comprising an insulation film buried at a side wall portion of the surface strap and formed of a material different from a material of the second oxide film.

4. The semiconductor memory device according to claim 1, further comprising a silicide layer formed on the gate electrode and the surface strap.

5. The semiconductor memory device according to claim 1, wherein the word line is provided in a transverse direction of the pillar, and the bit line is provided in a direction crossing the word line.

6. The semiconductor memory device according to claim 1, wherein the memory cells are arranged such that a pair of said MOSFETs and a pair of said trench capacitors are disposed adjacent to each other, and the paired MOSFETs and the paired trench capacitors are alternately arranged in a staggered fashion.

7. A method of fabricating a semiconductor memory device, comprising:

recess-etching a major surface of a semiconductor substrate, thereby forming a pillar that becomes a device formation region;

burying an insulation film in the recess-etched region, thereby forming a device isolation region;

forming at least a part of a gate insulation film on a surface of the pillar;

burying a gate electrode material at the device isolation region in the recess-etched region, thereby forming a gate electrode on a side wall and an upper surface of the pillar;

forming a trench in a vicinity of an end portion

of the pillar, and forming a capacitor on a side wall portion of the trench;

introducing impurities in the pillar using the gate electrode as a mask, thereby forming first and second activation regions such that the gate electrode is interposed between the first and second activation regions;

burying a first oxide film at a side wall of the pillar on the device isolation region such that the gate electrode is interposed;

forming a second oxide film on an upper part of the pillar;

removing an upper part of the first oxide film using the second oxide film as a mask, thereby exposing an upper surface and an upper part of the side wall of the pillar; and

forming a conductive material on the exposed upper surface and the exposed upper part of the side wall of the pillar, thereby forming a surface strap that electrically connects the capacitor and the second activation region.

8. The method of fabricating a semiconductor memory device according to claim 7, further comprising burying a third oxide film at a side wall portion of the surface strap, the third oxide film being formed of the same material as the second oxide film.

9. The method of fabricating a semiconductor

memory device according to claim 7, further comprising burying a first insulation film at a side wall portion of the surface strap, the first insulation film being formed of a material different from a material of the second oxide film.

10. The method of fabricating a semiconductor memory device according to claim 8, further comprising:

forming a second insulation film on the surface strap, following the formation of the surface strap;

forming a contact hole in the first and second insulation films at a position above the second activation region;

forming a bit line contact in the contact hole; and

forming a bit line on the second insulation film.

11. The method of fabricating a semiconductor memory device according to claim 7, further comprising:

exposing an upper part of the gate electrode, following the formation of the surface strap; and

forming a silicide layer on the gate electrode and the surface strap through a salicide process.

12. The method of fabricating a semiconductor memory device according to claim 11, further comprising:

forming a second insulation film on the silicide layer, following the formation of the silicide layer;

forming a contact hole in the first and second

insulation films at a position above the second activation region;

forming a bit line contact in the contact hole; and

forming a bit line on the second insulation film.

13. The method of fabricating a semiconductor memory device according to claim 7, wherein said burying of the second oxide film comprises burying an oxide film by coating.

14. The method of fabricating a semiconductor memory device according to claim 8, wherein said burying of the third oxide film comprises burying an oxide film by coating.